

## Process for manufacturing buried channels and cavities in semiconductor wafers

Patent Number: EP1049157

Publication date: 2000-11-02

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Requested Patent:  EP1049157

Application Number: EP19990830255 19990429

Priority Number(s): EP19990830255 19990429

IPC Classification: H01L21/764; H01L21/20

EC Classification: H01L21/20C, B81C1/00F2D4B, H01L21/764

Equivalents:  US6376291

Cited Documents: EP0890998; US4993143; US4771638

### Abstract

The process comprises the steps of forming, on a monocrystalline-silicon body (11), an etching-aid region (13) of polycrystalline silicon; forming, on the etching-aid region (13), a nucleus region (17) of polycrystalline silicon, surrounded by a protective structure (26) having an opening (22') extending as far as the etching-aid region (13); TMAH-etching the etching-aid region (13) and the monocrystalline body (11), forming a tub shaped cavity (30); removing the top layer (19) of the protective structure (26); and growing an epitaxial layer (33) on the monocrystalline body (11) and the nucleus region (17). The epitaxial layer, of monocrystalline type (33a) on the monocrystalline body (11) and of polycrystalline type (33b) on the nucleus region (17), closes upwardly the etching opening (22'), and the cavity (30) is thus completely embedded in the resulting wafer (34). 

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## Description

[0001] The present invention regards a process for manufacturing buried channels and cavities in semiconductor material wafers.

[0002] As known, presently numerous applications require channels or cavities inside a silicon substrate, for example for making suspended masses of microactuators and/or sensors of various kinds, such as speed, acceleration and pressure sensors, or for insulating electronic components.

[0003] At present, buried cavities can be made basically in two ways. According to a first solution, shown in Figure 1, two monocrystalline silicon wafers 1, appropriately excavated so as each of them presents a half-cavity, are bonded together using an adhesive layer (for example, silicon oxide 2) so that the two half-cavities form a buried cavity 3.

[0004] According to a second solution, shown in Figure 2, a wafer 1 of monocrystalline silicon, appropriately excavated so as to present final cavities 4, is bonded to a glass layer 5 (anodic bonding process).

[0005] Such solutions are costly, highly critical, have low productivity, and are not completely compatible with the usual technological phases involved in the manufacture of microelectronic components. In addition, in the solution of Figure 2, it is not always possible to make also an integrated circuit.

[0006] The aim of the present invention is thus to provide a process that eliminates the disadvantages of the known solutions.

[0007] According to the present invention, a process for manufacturing buried cavities in semiconductor material wafers and a semiconductor material wafer are provided, as defined in Claims 1 and 12, respectively.

[0008] For an understanding of the present invention, a preferred embodiment thereof is now described, as a non-limiting example, with reference to the attached drawings, wherein:

Figure 1 shows a cross section through a semiconductor material wafer made according to a known solution;

Figure 2 presents a cross section of another known solution;

Figures 3 to 11 show cross sections through a semiconductor material wafer in successive manufacturing steps, according to the present invention; and

Figure 12 shows, on a reduced scale, the wafer obtained with the manufacturing process according to the present invention.

[0009] Figure 3 shows a wafer 10 of monocrystalline silicon formed by a substrate 11 having a surface 12. On the surface 12 an etching-aid region 13 is formed, and has a thickness preferably comprised between 450 and 1000 nm; the etching-aid region 13 is obtained, for example, by chemical vapour deposition (CVD) of a polycrystalline silicon layer and subsequent definition of the polycrystalline silicon layer, using a resist mask. The etching-aid region 13 has the function of modifying the shape of the desired cavities or channels, as explained hereinafter.

[0010] Subsequently, a thermal oxidation is carried out (Figure 4); a first pad layer 15 of silicon oxide is then grown on the etching-aid region 13 and on the surface 12 of the wafer 10 where the latter is not covered by the etching-aid region 13. The first pad layer 15 has, for example, a thickness comprised between 20 and 100 nm. Thereafter a first etch-shielding layer 16 of silicon nitride having a thickness, for example, comprised between 90 and 200 nm, and then a nucleus layer 17 of polycrystalline silicon having a thickness comprised between 1 and 2  $\mu$ m are deposited. The nucleus layer 17 is preferably deposited by CVD. A thermal oxidation is then carried out, forming a second pad layer 18 of silicon oxide, having a thickness comprised, for example, between 20 and 60 nm, on the nucleus layer 17; and then a second etch-shielding layer 19 of silicon nitride is deposited, and has a thickness comprised, for example, between 90 and 200 nm. In this way, the intermediate structure of Figure 4 is obtained, which presents a stack of

layers 16-19.

[0011] A resist mask 20 is then formed (Fig. 5) and covers the entire wafer 10, except for a window 21 above the etching-aid region 13. Using the resist mask 20, the second etch-shielding layer 19, the second pad layer 18, the nucleus layer 17, and the first etch-shielding layer 16 are etched in succession by dry and wet etchings. Etching ends automatically on the first pad layer 15. At the end of etching, a hole 22 extends through the stack of layers 16-19 down to the first pad layer 15. Advantageously, the width of the hole 22 is comprised between 1 and 5  $\mu$ m, and its length and shape (in the direction perpendicular to the plane of the drawing) are determined by the length and shape of the etching-aid region 13 and, ultimately, by the desired characteristics of the cavity to be made.

[0012] Subsequently (Fig. 6), the resist mask 20 is removed, and the exposed surface of the nucleus layer 17 facing the hole 22 is thermally oxidized and forms an oxide portion 24 having a thickness comprised between, for example, 20 and 100 nm and joining to, without solution of continuity, the second pad layer 18.

[0013] A third etch-shielding layer 25 of silicon nitride is then deposited and has a thickness comprised preferably between 90 and 200 nm (Fig. 7) and completely coats the walls and the bottom of the hole 22. The third etch-shielding layer 25 is then anisotropically etched and is removed in the horizontal portions on the second etch-shielding layer 19 and on the bottom of the hole 22. A coating region 25' remains on the lateral walls of the hole (now indicated with 22') and joins, without solution of continuity, with the first and second etch-shielding layers 16, 19, also of silicon nitride, forming with the latter a protective structure 26, which completely envelops the second nucleus layer 17 (Fig. 8).

[0014] Next, the uncovered portion of the first pad layer 15, beneath the hole 22', is dry or wet etched, in a time controlled way, uncovering the etching-aid region 13. The intermediate structure shown in Fig. 8 is thus obtained.

[0015] The substrate 11 is then etched, in a time controlled way, using tetramethylammoniumhydroxide (TMAH) having the formula  $(CH_3)_4NOH$  (Fig. 9). The shape of the etching is determined by both the presence of the etching-aid region 13 and the etch directionality. In fact, since the etching-aid region 13 is of polycrystalline silicon, it is removed preferentially with respect to the substrate 11, which is of monocrystalline silicon, and determines the etch extent, parallel to the surface 12. On the other hand, with the structure of Fig. 9, where the surface 12 of the wafer has orientation  $\langle 100 \rangle$ , the oblique etching speed, according to the orientation  $\langle 100 \rangle$ , is much lower than the etching speed according to the orientation  $\langle 110 \rangle$ , and the monocrystalline silicon of the substrate 11 is preferentially etched along the vertical.

[0016] It follows that, on the whole, etching occurs according to fronts having a width determined by the progressive removal of the etching-aid region 13, and extends in depth into the substrate 11, as shown in Figure 9, where the dashed lines and the dashed and dotted lines indicate successive etching fronts, and the arrows indicate the etching advancement direction. At the end of etching, after a preset time, dependent on the width of the etching-aid region 13, a tub shaped cavity 30 is formed in the substrate 11. In this step, the nucleus layer 17 is protected by the protective structure 26.

[0017] The wall of the cavity 30 is then thermally oxidized and forms a protective layer 31 (Fig. 10) having a thickness preferably comprised between 60 and 300 nm.

[0018] Subsequently (Fig. 11), the nitride material is etched, removing the second etch-shielding layer 19, and then the second oxide pad layer 18 is etched. Given the greater thickness of the protective layer 31, as compared to the second pad layer 19, in this step the protective layer 31 is, at most, removed only partially.

[0019] Using a resist mask, the nucleus layer 17 is suitably shaped so as to be removed everywhere, except above and around the cavity 30; in addition, the first etch-shielding layer 16 and the first pad layer 15 are etched and removed where they are exposed. Consequently, the surface 12 of the substrate 11 is once more exposed, except for at the cavity 30.

[0020] Finally (Fig. 12), epitaxial growth is carried out starting from the substrate 11 (where this is not covered) and from the nucleus layer 17. In particular, a so-called pseudo-epitaxial layer 33 is formed, formed by a monocrystalline portion 33a on the substrate 11 and a polycrystalline portion 33b on the

nucleus layer 17, these portions being separated by a transitional region 33c, as shown in Figure 12. The substrate 11 and the pseudo-epitaxial layer 33 thus form a wafer 34. In addition, the epitaxial growth over the nucleus layer 17 takes place also horizontally, closing the hole 22'. Consequently, the cavity 30 is closed on all its sides and is completely embedded in the wafer 34.

[0021] The wafer 34 then undergoes further processing steps according to the devices to be made. In particular, in the polycrystalline portion 33b suspended structures are made, such as membranes, induction coils, accelerometers, etc., and in the monocrystalline portion 33a of the pseudo-epitaxial layer 33 electronic processing and control components are integrated.

[0022] The advantages of the described process are the following: first, the process enables forming closed cavities in a silicon wafer with process steps that are fully compatible with semiconductor manufacturing processes. The process does not present particular critical aspects, and enables good productivity, contained costs, and the integration of microstructures and electronic components.

[0023] Finally, it is clear that modifications and variations can be made to the process described and illustrated herein, all of which fall within the scope of the invention, as defined in the attached claims. In particular, the size, shape and number of holes 22' are suitably chosen on the basis of the size and shape of the cavity 30 to be formed and of the characteristics of the TMAH etching on the substrate 11. In particular, in the case of a hole 22' of an elongated shape, it is possible to obtain elongated channels; in the case of suspended structures of large area, it is possible to make a number of holes 22' above a same etching-aid region 13 so as to form a number of initial cavities which then join up to form a final, large size cavity parallel to the surface 12 of the substrate 11.

[0024] In addition, the thermal oxidation used to form the protective layer 31 may be omitted, and the nucleus layer 17 can be made in two steps by depositing a thin vapour-phase layer and then growing a polycrystalline layer epitaxially up to the desired thickness.

[0025] Finally, after forming the cavity 30, the removal of the second etch-shielding layer 19 and of the second pad layer 18 can be carried by wet etching, also removing the coating region 25' and the oxide portion 24.

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## Claims

1. A process for manufacturing buried cavities in semiconductor material wafers, characterized by the steps of:

forming, on a monocrystalline body (11) of semiconductor material, a nucleus region (17) surrounded by a protective structure (26);  
forming a cavity (30) in said monocrystalline body (11) beneath said nucleus region (17);  
removing at least a top portion (19) of said protective structure (26); and  
growing an epitaxial layer (33) on said monocrystalline body (11) and said nucleus region (17).

2. A process according to Claim 1, characterized in that said step of forming a cavity (30) comprises the step of etching said monocrystalline body (11) through an opening (22') delimited by said protective structure (26).

3. A process according to Claim 1 or Claim 2, characterized in that said etching step is carried out by TMAH-etching.

4. A process according to any of Claims 1-3, characterized in that, before said step of forming a nucleus region (17), the step is carried out of forming an etching-aid region (13) directly on said monocrystalline body (1), said etching-aid region being arranged beneath said nucleus region (17) and being separated from said nucleus region (17) by said protective structure (26).

5. A process according to Claim 4, characterized in that said etching-aid region (13) is of polycrystalline silicon.

6. A process according to Claim 4 or 5, characterized in that said step of forming a nucleus region (17) comprises the steps of:

forming, on said monocrystalline body (11) and said etching-aid region (13), a layer stack (16-19) comprising a first etch-shielding layer (16), a polycrystalline-silicon layer (17), and a second etch-shielding layer (19);  
forming, in said layer stack and on said etching-aid region (13), a window (22) having side delimiting walls; and  
coating said side delimiting walls of said window with a coating region (25'), forming an opening (22') for etching said monocrystalline body (11).

7. A process according to Claim 6, characterized in that said first and second etch-shielding layers (16, 19) and said coating region (25') are of silicon nitride.

8. A process according to Claim 7, characterized by the step of forming a thermal oxide layer (15, 18) beneath said first and second etch-shielding layers (16, 19) and forming thermal oxide regions (24) beneath said coating region (25').

9. A process according to any of the foregoing Claims, characterized by the step of forming a protective region (31) on walls of said cavity (30), before removing a top portion (19) of said protective structure (26).

10. A process according to Claim 9, characterized in that said step of forming a protective region (31) comprises the step of thermally oxidizing said walls of said cavity (30).

11. A process according to any of Claims 1-10, characterized in that said step of growing an epitaxial layer (33) comprises forming a monocrystalline region (33a) on said monocrystalline body (11), and a polycrystalline region (33b) on said nucleus region (17).

12. A wafer (34) of semiconductor material, characterized in that it comprises at least one buried cavity (30)

formed in a monocrystalline region (11) and closed at the top by an epitaxial layer (33) comprising a polycrystalline portion (33b) above said buried cavity (30) and a monocrystalline region (33a) on said monocrystalline region (11).

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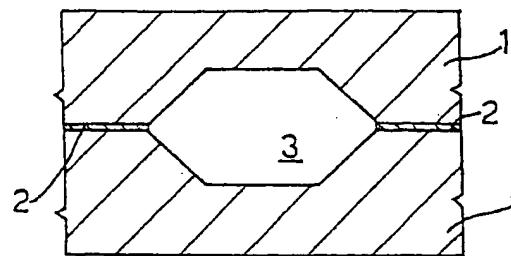


Fig.1

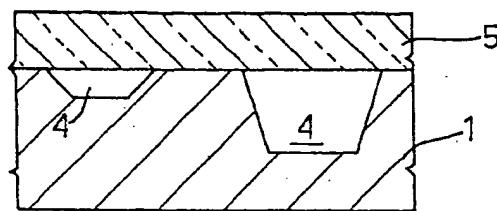


Fig.2

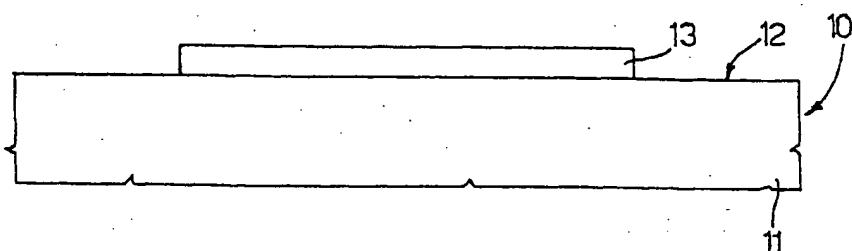


Fig.3

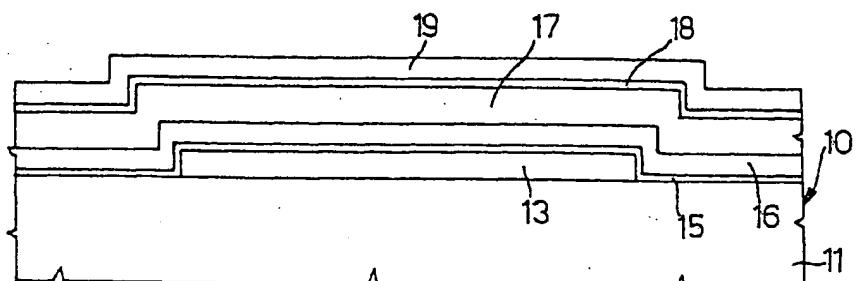


Fig.4

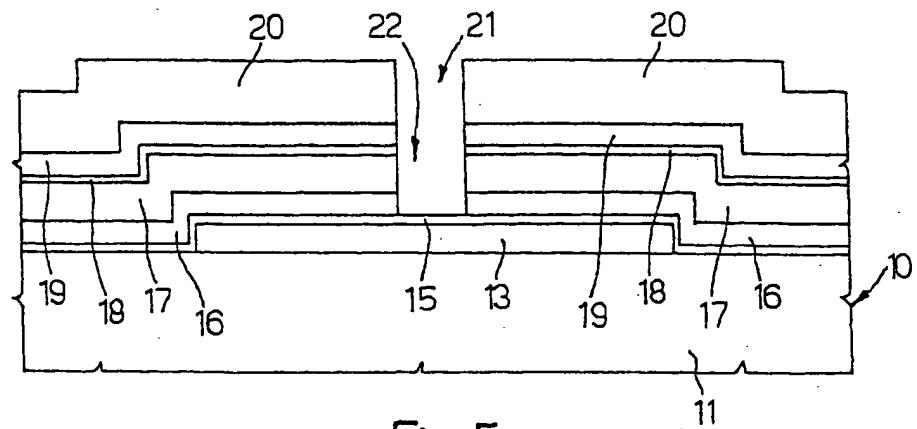


Fig. 5

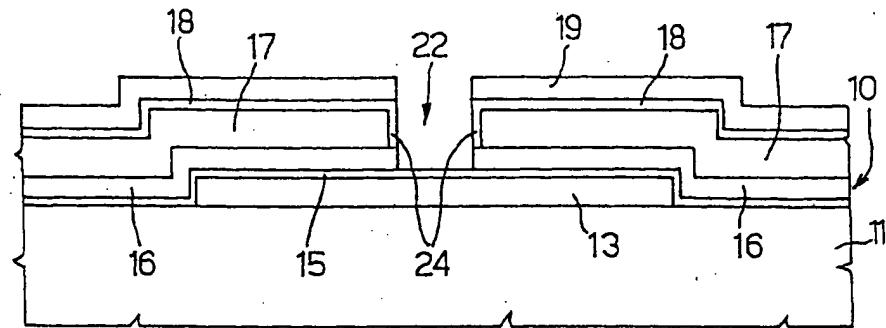


Fig. 6

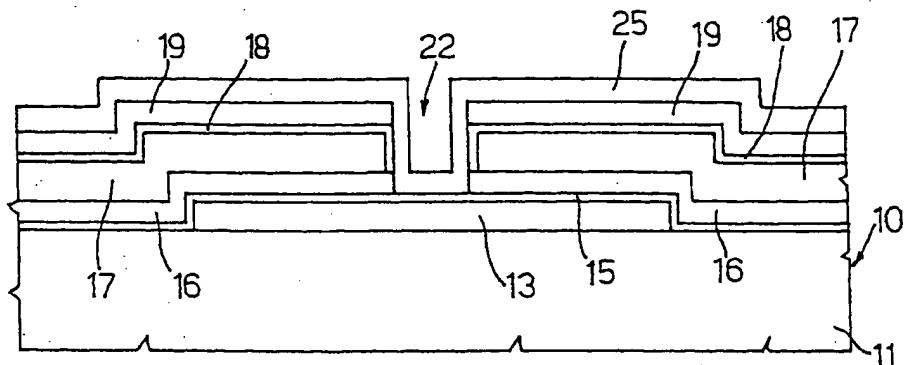


Fig. 7

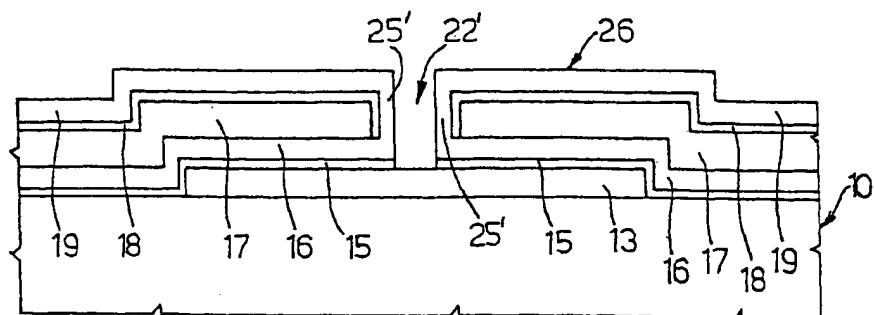


Fig. 8

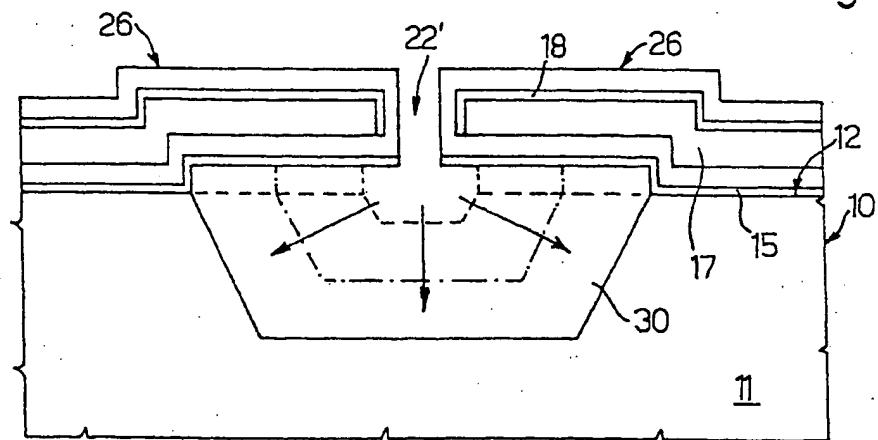


Fig. 9

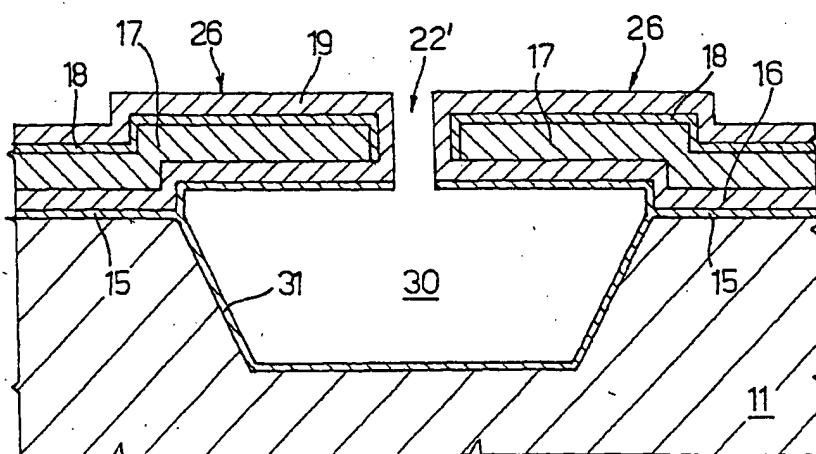


Fig. 10

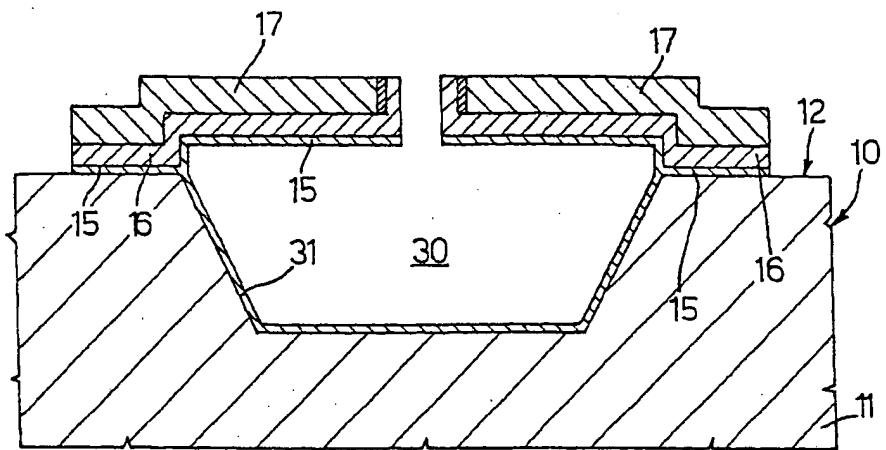


Fig.11

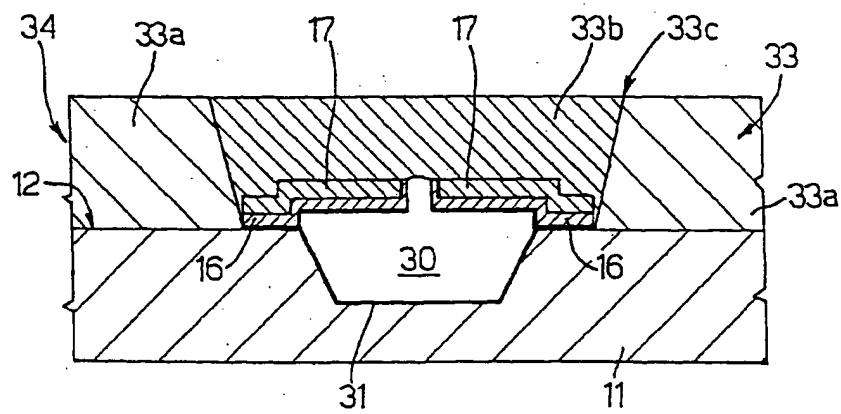


Fig.12